ASD IC for the Thin Gap Chambers in the LHC Atlas Experiment

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Abstract
An amplifier-shaper-discriminator (ASD) chip was designed and built for Thin Gap Chambers in the forward muon trigger system of the LHC Atlas experiment. The ASD IC uses SONY Analog Master Slice bipolar technology. The IC contains 4 channels in a QFP48 package. The gain of its first stage (preamplifier) is approximately 0.8V/pC and output from the preamplifier is received by a shaper (main-amplifier) with a gain of 7. The baseline restoration circuit is incorporated in the main-amplifier. The threshold voltage for discriminator section is common to the 4 channels and their digital output level is LVDS-compatible. The IC also has analog output of the preamplifier. The equivalent noise charge at input capacitance of 150 pF is around 7500 electrons. The power dissipation with LDVS outputs (100 Ω load) is 59mW/ch.

I. INTRODUCTION
The Atlas experiment in the LHC uses Thin Gap Chambers (TGC) \([1,2]\) as its forward muon trigger detectors \([3,4]\). Forward-going muon tracks are bent by a magnetic field generated by a toroidal coil and pass through the TGCs where their momenta are measured for level-1 trigger. There will be a triplet TGC wheel followed by two wheels of TGC doublets, totaling 7 layers of TGCs per side. The total number of TGCs are 3600 and we will be dealing with TGC signals from their anodes (several wires are ganged together) and strips, totaling nearly 400k channels. Since the machine cycle of the LHC is 40MHz, the bunch crossing identification capability is mandatory for the electronics and the detector to provide the trigger and readout processing. Due to this requirement, TGCs, chambers with thin gap and narrow wire spacing are adopted to the forward muon trigger detector. However this chamber structure introduces large detector capacitance. The capacitance of the TGC as a signal source is a few hundred pF, which comes from the thin gap structure of the chamber and is rather large capacitance when compared with that of an ordinary chamber. The requirement of fast signal processing and the characteristic of large detector capacitance contradict each other when we design a low-noise preamplifier. Much attention was paid to the process choice and circuit design for the TGC application. Since about 400k channels are required, reliability and cost are of the utmost concern. In short, the ASD IC as TGC front-end electronics must have a good time resolution for bunch-crossing identification and a high rate capability to cope with high background rate (100 kHz /channel) and must be robust for the longtime operation without maintenance.

II. CIRCUIT DESIGN
A. Technology Choice
Because the signal source has relatively large capacitance and because fast signal shaping as well as low noise are the requirements on the amplifiers, transistors with large \(g_m\) are preferred. Hence we chose to base the amplifiers on bipolar transistors \([5,6]\). The chip has been developed in collaboration with SONY Corporation, using their bipolar ‘Analog Master Slice Process’. This semi-custom process provides prefabricated NPN and PNP transistors, resistors and capacitors, so that a designer has to design using these elements that are predetermined beforehand for the silicon wafer. The base-structure we used contains 850 NPN transistors, 3834 PNP transistors, 1738 resistors and 42 capacitors, totaling approximately 1000 usable elements. There are five kinds of NPN transistors on the chip including low noise transistors and power transistors. The standard transistor has \(f_T=3.2\ GHz\). The low noise transistor has \(f_T=950\ MHz\) and base-spread resistance \(r_{bb'}=17.5\ Ω\).

Figure 1: Block Diagram of the ASD chip
Availability of the low-noise transistors with very low $r_{bb'}$ was one of the motivation to use the process. There also are two kinds of PNP transistors of which the standard one has $f_T=300$ MHz. Capacitors are of 2 pF and 20 pF value totaling 408 pF (Metal Insulator Semiconductor, MIS capacitor) in total. Resistors are of either 8 kΩ or 2.5 kΩ (poly-silicon), 297 Ω (diffused) and 129 Ω (diffused).

### B. Circuit Diagram

A block diagram of the ASD chip is shown in Figure 1, with schematics in Figure 2 and 3. Its first stage is a common-emitter cascade charge amplifier. The input stage of the preamplifier is implemented with the low-noise NPN transistor with $r_{bb'}$ of 17.5 Ω. The relatively large capacitance (higher than 10 pF between the collector and substrate) of the transistor disfavors the use of the transistor in common-base configuration which is usually employed in preamplifiers for chambers [7,8]. The collector current of the head transistor is set high (0.9 mA) to achieve large $g_{m}$, which have advantage to achieve lower noise at large detector capacitance. The integration constant is set to 16 ns. The gain of the preamplifier stage is approximately 0.8 V/pC. An emitter follower output of this preamplifier stage is provided for monitoring.

The second stage consists of a main-amplifier with a baseline restorer and differential outputs. The main-amplifier section has a gain of 7. Depending upon the output differential signal level seen by the switch control section, the switch connects to the “A” side or to the “B” side of Figure 1. When the switch is connected to the “A” side, the capacitor $C_b$ will be charged from the current source by the amount of ‘$i$’. When the switch is connected to the ‘B’ side, the capacitor will be discharged by the amount ‘$i$’, resulting in stabilized DC output levels, or a baseline restoration. In other words, the circuit makes the baseline level of the differential outputs from the main-amplifier to be equal.

Following the main-amplifier is an offset setting which transforms the main-amplifier outputs to the levels required at the inputs to the comparator, where offset voltage is controlled by DC voltage ($V_{th}$) supplied from outside of the chip. The comparator is shown in Figure 3. Its outputs conform to the Low Voltage Differential Signalling standard, LVDS, to assure drivability and immunity against noise and minimizing power.
By design, this circuit can be used for both wire and strip signals by setting an appropriate threshold level. Table 1 is a summary of this chip’s characteristics.

Table 1: TGC ASD chip characteristics

<table>
<thead>
<tr>
<th>Process</th>
<th>SONY Analog Master Slice</th>
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</thead>
<tbody>
<tr>
<td>Specification</td>
<td>bipolar semi-custom</td>
</tr>
<tr>
<td></td>
<td>preamplifier with a gain of 0.8 V/pC</td>
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<tr>
<td></td>
<td>16 nsec integration time</td>
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<td></td>
<td>input impedance of around 80 Ω</td>
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<tr>
<td></td>
<td>open-emitter analog output</td>
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<tr>
<td></td>
<td>main-amplifier with a gain of 7</td>
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<td></td>
<td>baseline restoration circuits</td>
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<tr>
<td></td>
<td>comparator with LVDS outputs</td>
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<tr>
<td></td>
<td>ENC ~ 7500 electrons at C_d = 150 pF</td>
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<tr>
<td></td>
<td>4 channels in a QFP48 plastic package</td>
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<tr>
<td></td>
<td>threshold voltage common for all 4 channels</td>
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<td></td>
<td>required voltage : +/- 3V, GND</td>
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<td></td>
<td>59 mW/ch when driving a 100 Ω load</td>
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<td></td>
<td>(46 mW in ASD chip and 13 mW at LDVS receiver end)</td>
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</tbody>
</table>

Figure 5: Calculated ENC as a function of detector capacitance

C. Simulation

Figure 4 shows the result of a PSPICE simulation of the preamplifier output, the main-amplifier differential outputs and the comparator LVDS outputs against impulse inputs of -0.1 ~ -0.5 pC charge. Dynamic range (non-saturated range) of the preamplifier is negative / positive impulse charge input of from -1.2 to +2.0 pC. The slewing rate of the preamplifier also limits the linearity for large positive charge inputs. The dynamic range and the gain of the preamplifier observed at the buffered direct output depends on the external load and is less than the internal one. The circuit can successfully accept signals of 5 MHz or higher frequency. Figure 5 shows the calculated equivalent-noise-charge (ENC) as a function of detector capacitance. At 150 pF input capacitance, ENC is 7500 electrons r.m.s., The input impedance is around 80 Ω for input signals of up to 100 MHz.

D. IC Layout

4 channels of ASDs was fabricated on a 3.1mm X 3.1mm die shown in Figure 6. The threshold voltage is common to 4 channels. In the layout work of the IC, we paid much attention to reduce interference between analog and digital signals and cross-talk among channels. Both ground and power patterns and I/O pads for the analog part are separated from those for the digital part. The chip is housed in a QFP48 package. The pins of the package were assigned keeping right-left symmetry, that would make the designing of the PC board layout easier. For the protection from static charge, diodes are attached between all I/O pads and the most positive / negative voltage excepting those for ground and DC powers.

III. PERFORMANCE

The analog and digital signals from the ASD chip for impulse inputs from -0.1 to -0.5 pC are shown in Figure 7. The overall time walk of the comparator outputs due to the input charge variation of between -0.1 pC to -2 pC is less than 2 ns, when the threshold is set at 0.01 pC equivalent,
as shown in Figure 8.

We also tested the performance of the main-amplifier and comparator using prototype chips where the preamplifier, the main-amplifier and the comparator were fabricated separately for independent study. In order to check comparator characteristics, we measured propagation delay while changing conditions such as: varying over-the-threshold-voltage of the input pulse that has fixed rise time / varying over-the-threshold-voltage of the input pulse that has fixed slope / varying rise time while input pulse height was kept constant. The result show that the time walk of the comparator was within less than 2 ns under these conditions. These results agree with predictions by the PSPICE.

Temperature dependence of the preamplifier gain was approximately -0.08 %/°C. The feedback capacitor of the preamplifier is supposed to be the major contributor to temperature dependence.

The ENC was measured as a function of the input capacitance as shown in Figure 9. We calculated the ENC using design parameters of the preamplifier and measured impulse response of the evaluation system. The calculation reproduces the measured data with the \( r_{bb'} = 15 \) Ω and the \( h_{fe} = 90 \). Cross-talk among channels were less than 0.5 % when analog output pins are left open. If the open-emitter buffer for the analog output drives 50 Ω load, the cross-talk became 3 times larger. Influence of the digital part on the analog part was much less than the cross-talk between channels.

**Figure 7:** analog and digital signals from the ASD for impulse inputs from -0.1 to -0.5 pC.

**Figure 8:** Overall time walk of the ASD outputs due to the input charge variation.

**Figure 9:** Measured the ENC (closed circle) and calculated ENC (open circle) using design parameters of the preamplifier and measured impulse response of the evaluation system.

**IV. SUMMARY**

We have designed and built a chip containing 4 channels of ASDs for the TGCs of the Atlas LHC experiment using SONY semi-custom Analog Master Slice bipolar process. Produced pre-production samples (1200 of them) performed to the specification. We also developed 16-channel ASD boards and performed beam tests with real TGCs at both KEK and CERN in 1998. Irradiation test using gamma ray and
neutrons were performed and then radiation tolerance of the chip has been assured. New masks for the mass production was produced for the mass-production. The inspection setup to be used at the production line in SONY was designed and built. The mass-production (100k pieces) of the chips is scheduled in 1999.

V. ACKNOWLEDGMENT

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VI. REFERENCES


